UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,462	07/07/2003	Tzu-Chiang Sung	252011-1490	7583

47390 7590 04/18/2006

THOMAS, KAYDEN, HOSTEMEYER & RISLEY LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,462	SUNG ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,7-11,13,15-17,19,21-25,27 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7-11,13,15-17,19,21-25,27 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3, 5, 15-17, 19, and 29-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Hebert (US PGPub 2002/0117714).

Regarding claims 1, 15, and 29, Figures 2H-2J and 5 of Hebert disclose a substrate 52; first and second wells (54 and 60/66B, respectively) respectively of a first type (N) and a second type (P) in the substrate; a gate (62/68A/68B) formed on a junction between the first and second wells, without a field oxide adjacent to the gate and between the gate and the first and second wells; first and second doped regions (70A and 70B, respectively) both of the second conductivity type, respectively formed in the first and second wells and on both sides of the gate; a third doped region 69 of the first type in the first well and adjacent to the first doped region; and a fourth lightly doped region 66A (see Figures 2H-2J) of the second type adjacent to the first doped region and beneath the gate, wherein the fourth lightly doped region is shallower than the first doped region. Regarding claim 15, the above device must be made by the claimed method.

Regarding claims 2, 16, and 30, Figure 5 of Hebert discloses field oxides (58A and 58B) isolating the high voltage device from other devices on the substrate.

Regarding claims 3, 17, and 31, Figures 2J and 5 of Hebert discloses a gate oxide 55 on the substrate, a conducting layer 62 on the gate oxide and spacers (68A and 68B) on two sides of the gate oxide and conducting layer.

Regarding claims 5, 19, and 32, Figure 5 of Hebert discloses there is a spacing of the second doped region 70B to the gate.

Regarding claims 7, 21, and 33, Figure 6 of Hebert discloses an alternative embodiment, which is the same as the embodiment discussed above in relation to Figure 5, except the conductivity types are reversed. Therefore, the first and second types are respectively P and N types. Note that Hebert discloses p-body region 390 can be a p-well (paragraph [0061]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 22, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert in view of Williams et al. (US Pat. 5,514,608, hereinafter Williams).

Regarding claims 8, 22, and 34, Figure 5 of Hebert discloses the first and second types are respectively N and P types. The difference between Hebert and the claimed invention is an N+ buried layer in the substrate and beneath the first and second wells. Figure 5 of Williams discloses a LDMOS transistor with a buried layer 504 beneath a gate 509 and first and second

wells (503 and N-drift, respectively), wherein the buried layer has the opposite conductivity type as that of the source and drain regions (502 and 507, respectively). Note that Williams discloses the conductivity types shown in Figure 5 can be reversed (col. 9, lines 39-44), meaning the buried layer is n-type. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Hebert by including an N+ buried layer for the purposed of increasing the breakdown voltage (col. 2, lines 55-59 of Williams).

Claims 9-11, 13, 23-25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert in view of Ito et al. (US Pat. 5,856,695, hereinafter Ito) and Williams.

Regarding claims 9 and 23, Figures 2H-2J and 5 of Hebert disclose a high voltage device formed on a P substrate 52 comprising: a HVPMOS comprising: P and N wells (66B/60 and 54, respectively) in the substrate; a gate (62/68A/68B) formed on a junction between the first P and N wells, without a field oxide adjacent to the second gate and between the gate and the P and N wells; two P+ doped regions (70B and 70A) respectively formed in the P and N wells and on both sides of the first gate; an N+ doped region 69 in the N well and adjacent to the P+ doped region 70A in the N well; and a P lightly doped region 66A adjacent to the P+ doped region in the N well and beneath the gate. A difference between Hebert and the claimed invention is an HVNMOS device formed in the P substrate, wherein the HVNMOS has essentially the same structure but opposite conductivity types. Figure 23 of Ito discloses both an HVNMOS and an HVPMOS formed on a P substrate, wherein the HVNMOS and HVPMOS have essentially the

same structure but opposite conductivity types. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Hebert by including an HVNMOS having the same structure as that of the HVPMOS (but oppositely doped) on the P substrate as taught by Ito. The ordinary artisan would have been motivated to further modify Akaishi in the manner described above for the purpose of increasing integration density while increasing the versatility of the device (by forming a CMOS device). The advantage of CMOS devices is well known in the art. A further difference between Hebert and the claimed invention is having an N+ buried layer in HVPMOS device. Figure 5 of Williams discloses a LDMOS transistor with a buried layer 504 beneath a gate 509 and first and second wells (503 and N-drift, respectively), wherein the buried layer has the opposite conductivity type as that of the source and drain regions (502 and 507, respectively). Note that Williams discloses the conductivity types shown in Figure 5 can be reversed (col. 9, lines 39-44), meaning the buried layer is n-type. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Hebert by including an N+ buried layer for the purposed of increasing the breakdown voltage (col. 2, lines 55-59 of Williams'608). Regarding claim 23, the above device must be made by the claimed method.

Regarding claims 10 and 24, Figure 5 of Hebert discloses field oxide regions (58A and 58B) isolating the devices from other devices on the substrate.

Regarding claims 11 and 25, Figures 2J and 5 of Hebert discloses a gate oxide 55 on the substrate, a conducting layer 62 on the gate oxide and spacers (68A and 68B) on two sides of the gate oxide and conducting layer.

Regarding claims 13 and 27, Figure 5 of Hebert discloses there is a spacing of the second doped region 70B to the gate.

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

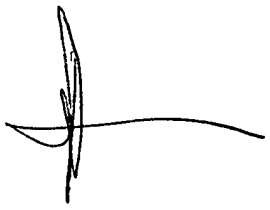
Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Matthew C. Landau

April 7, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER